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Mitigation of Power Quality Issues by Nine Switches UPQC Using PI & ANN with Hysteresis Control

D. Uma Maheswara Rao[1], K. Sravanthi[2], Avinash Vujji[3], K. Durga Syam Prasad[4]

[1] P.G Student, Department of EEE, DIET College Of Engineering, Visakhapatnam- 531 002
[2]Assistant Professor, Department of EEE, Vignan's Institute of Engineering, Visakhapatnam- 531 002
[3] Sr.Assistant Professor, Department of EEE, DIET College Of Engineering, Visakhapatnam- 531 002
[4]Sr.Assistant Professor, Department of EEE, DIET's Institute of Engineering, Visakhapatnam- 531 002

Abstract
A nine-switch power converter having two sets of output terminals was recently proposed in place of the traditional back-to-back power converter that uses 12 switches in total. The nine-switch converter has already been proven to have certain advantages, in addition to its component saving topological feature. Despite these advantages, the nine-switch converter has so far found limited applications due to its many perceived performance tradeoffs like requiring an oversized dc-link capacitor, limited amplitude sharing, and constrained phase shift between its two sets of output terminals. Instead of accepting these tradeoffs as limitations, a nine-switch power conditioner is proposed here that virtually "converts" most of these topological short comings into interesting performance advantages. Aiming further to reduce its switching losses, Harmonics, Voltage Sag & Swell an appropriate discontinuous modulation scheme is proposed and studied here in detail to doubly ensure that maximal reduction of commutations is achieved. With an appropriately designed control scheme with PI and ANN with Hysteresis controller then incorporated, the nine-switch converter is shown to favorably raise the overall power quality in Simulation, hence justifying its role as a power conditioner at a reduced cost.

Index Terms—Discontinuous pulse-width modulation, nine switch converter, power conditioner, power quality.

I. INTRODUCTION

Since its first introduction, static power converter development has grown rapidly with many converter topologies now readily found in the open literature. Accompanying this development is the equally rapid identification of application areas, where power converters can contribute positively toward raising the overall system quality [1], [2]. In most cases, the identified applications would require the power converters to be connected in series [3] or shunt [4], depending on the operating scenarios under consideration. In addition, they need to be programmed with voltage, current, and/or power regulation schemes so that they can smoothly compensate for harmonics, reactive power flow, unbalance, and voltage variations. For even more stringent regulation of supply quality, both a shunt and a series converter are added with one of them tasked to perform voltage regulation, while the other performs current regulation. Almost always, these two converters are connected in a back to-back configuration [5], using 12 switches in total and sharing a common dc-link capacitor, as reflected by the configuration drawn in Fig. 1(a). Where available, a micro source can also be inserted to the common dc link, if the intention is to provide for distributed generation in a micro grid [6], without significantly impacting on the long proven proper functioning of the back-to-back configuration.

Even though facing no major operating concerns at present, improvements through topological modification or replacement of the back-to-back configuration to reduce its losses, component count, and complexity would still be favored, if there is no or only slight expected tradeoff in performance. A classical alternative that can immediately be brought out for consideration is the direct or indirect matrix converter, where 18 switches are used in total. That represents six switches more than the back-to-back configuration, but has the advantage of removing the intermediate electrolytic capacitor for compactness and lifespan extension. If the heavy switch count is still of concern, those indirect sparse matrix converters proposed in [7], [8] can be considered, where the minimum switch count attainable is nine, but at the expense of supporting only unidirectional power flow. Neither storage capacitor nor dc microsource is again needed, which thus renders the normal and sparse matrix converters as not the preferred choice, if ride-through is a requirement. Matrix converters are also not preferred, if voltage buck and boost operations are both needed for a specified direction of power flow.

Yet another reduced semiconductor topology can be found in [9], where the B4 converter is introduced for dc–ac or ac–dc energy conversion. The B4 converter uses four switches to form two phase legs with its third phase drawn from the midpoint of a split dc capacitive link. For tying two ac systems together, two B4 converters are needed with their split dc link shared [10]. The total number of switches needed is thus 8, which probably is the minimum achievable for interfacing two ac systems. The resulting ac–dc–ac converter should then be more rightfully referred to as the B8 converter. The B8 converter is, however, known to suffer from large dc-link voltage variation, unless both systems are of the same frequency and synchronized so that no fundamental current flows through the dc link. That certainly is a constraint, in addition to the lower ac voltage that can be produced by each B4 converter from its given dc-link voltage.

Overcoming some limitations of the B8 converter is the five leg converter introduced in [11], which conceptually can be viewed as adding a fifth phase leg to the B8 converter. The added phase leg is shared by the two interfaced ac systems with now no large fundamental voltage variation observed across its dc link. The only constraint here is the imposition of common frequency operation on the two interfaced ac systems, which then makes it unsuitable for applications like utility powered adjustable speed drives and series-shunt power conditioners.

Presenting a better reduced semiconductor alternative for high quality series–shunt compensation, this paper proposes a single stage integrated nine-switch power conditioner, whose circuit connection is shown in Fig. 1(b). As its name roughly inferred, the proposed conditioner uses a nine-switch converter with two sets of output terminals, instead of the usual 12 switch back-to back converter. The nine-switch converter was earlier proposed in [12] and [13] at about the same time, and was recommended for dual motor drives [14], rectifier–inverter systems, and uninterruptible power supplies [15]. Despite functioning as intended, these applications are burdened by the limited phase shift and strict amplitude sharing enforced between the two terminal sets of the nine-switch converter.

More importantly, a much larger dc-link capacitance and voltage need to be maintained, in order to produce the same ac voltage amplitudes as for the back-to-back converter. Needless to say, the larger dc-link voltage would overstress the semiconductor switches unnecessarily, and might to some extent overshadow the saving of three semiconductor switches made possible by the nine-switch topology. The attractiveness of the nine-switch converter, if indeed any, is therefore not yet fully brought out by those existing applications discussed in [13]–[15]. Although follow-up topological extensions can subsequently be found in [16], where a Z-source network and alternative modulation schemes are introduced, they did not fully address those critical limitations faced by the nine-switch converter, and not its traditional back-to-back counterpart.

Investigating further by taking a closer view at those existing applications described earlier, a general note observed is that they commonly use the nine-switch converter to replace two shunt converters connected back-to-back. Such replacement will limit the full functionalities of the nine-switch converter, as explained in Section II. In the same section, an alternative concept is discussed, where the nine-switch converter is chosen to replace a shunt and a series converter found in an integrated power conditioner, instead of two shunt converters. Underlying operating principles are discussed comprehensively to demonstrate how such "series–shunt" replacement can bring forth the full advantages of the nine-switch converter, while yet avoiding those limitations faced by existing applications. Details explaining smooth transitions between normal and sag operating modes are also provided to clarify that the more restricted nine-switch converter will not underperform the more independent back-to back converter even for sag mitigation.

During voltage sags, the second set of control schemes also has the ability to continuously keep the load voltages within tolerable range. This sag mitigation ability, together with other conceptual findings discussed in this paper but not in the open literature, has already been verified in experiment with favorable results observed.

II. SYSTEM CONFIGURATION

Basic block diagram of UPQC is shown in Figure.1, where as the overall control circuit is shown in the Figure.2. The voltage at PCC may be or may not be distorted depending on the other non-linear loads connected at PCC. Here the assumption of the voltage at PCC is distorted. Two voltage source inverters are connected back to back, sharing a common dc link.[8-10]

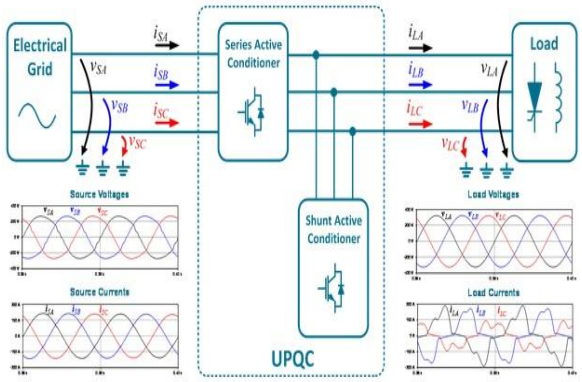

Figure.1 (a) Basic Block Diagram of conventional UPQC

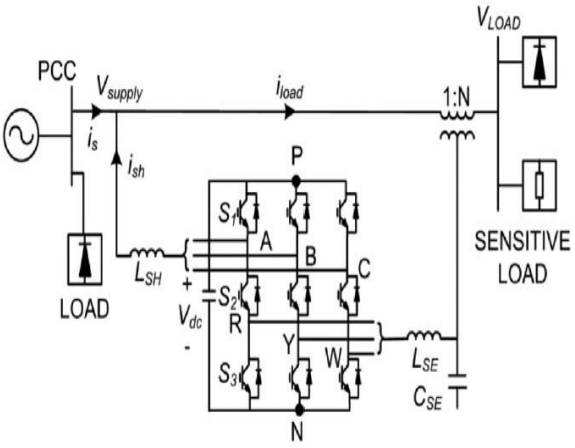

Figure1 (b) Basic Block Diagram of nine switch UPQC

One inverter is connected parallel with the load. It acts as shunt APF, helps in compensating load harmonic current as well as to maintain dc link voltage at constant level. The second inverter is connected in series with utility voltage by using series transformers and helps in maintaining the load voltage sinusoidal.[11-12]

As for the shunt active filter of the UPQC it is represented by $\frac{V_{dc}}{2}u_2$ with l_{sh} as the first order low-pass interfacing filter and r_{sh} as the losses of the shunt VSI. $\frac{V_{dc}}{2}u_2$ Represents the switched voltage across the shunt VSI output of the UPQC. The injection current of the shunt active filter is denoted by both u_1 and u_2 take the value of either -1 or 1 depending on the switching signal of the hysteresis control.

In Figure.2 the instantaneous current of the nonlinear load i_L is expanded into Different terms. The first term i_{Ljp} is the load Reference currents and voltages are generated using Phase Locked Loop (PLL) controller in UPQC.

III. OVERALL CONTROL CIRCUIT CONFIGURATION OF NINE SWITCH UPQC

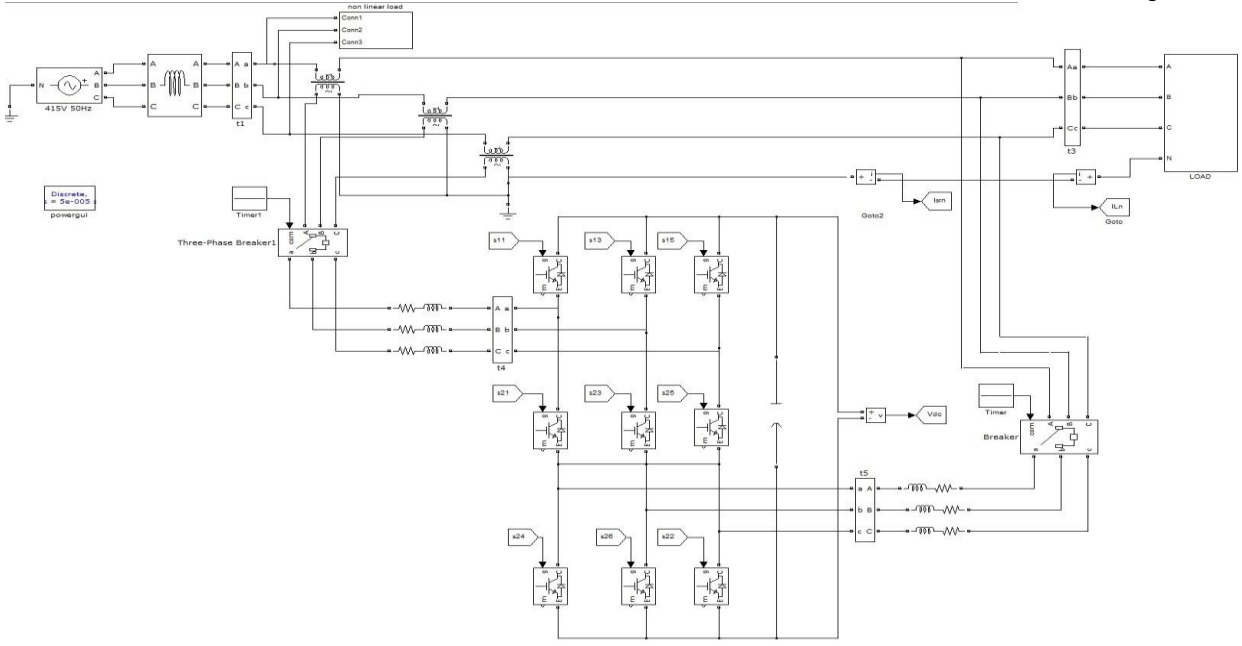

Figure.2 Overall Control Circuit Configuration of Nine Switch UPQC

The control strategy is based on the extraction of Unit Vector Templates from the distorted input supply. These templates will be then equivalent to pure sinusoidal signal with unity (p.u.) amplitude. The extraction of unit vector templates is

$$\left.\begin{aligned} U_a &= \sin(wt) \\ U_b &= \sin(wt-120) \\ U_c &= \sin(wt+120) \end{aligned}\right\} \quad (1)$$

Multiplying the peak amplitude of fundamental input voltage with unit vector templates of equation (1) gives the reference load voltage signals,

$$V^*_{abc} = V_m . U_{abc} \quad (2)$$

The error generated is then taken to a hysteresis controller to generate the required gate signals for series APF. The unit vector template can be applied for shunt Figure.3 Extraction of Unit Vector Templates and 3-Φ Reference Voltages shown in the Figure.3.The unit vector templates are generated APF to compensate the harmonic current generated by non-linear load. The shunt APF is used to compensate for current harmonics as well as to maintain the dc link voltage at constant level [13-14]. To achieve the above mentioned task.

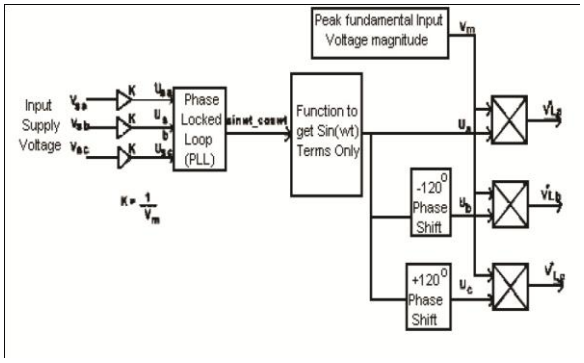

Figure.3 Extraction of Unit Vector Templates and 3-Φ Reference Voltages

The dc link voltage is sensed and compared with the reference dc link voltage. A PI controller then processes the error. The output signal from PI controller is multiplied with unit vector templates of equation (1) giving reference source current signals. The source current must be equal to this reference signal. In order to follow this reference current signal, the 3-phase source currents are sensed and compared with reference current signals. The error generated is then processed by a hysteresis current controller with suitable band, generating gating signals for shunt APF. The Nine Switch UPQC uses two back-to-back connected three phase VSI□s sharing a common dc bus. The hysteresis controller is used here to control the switching of the both VSI's.

IV. CONTROL STRATEGY OF NINE SWITCH UPQC

Nine Switch UPQC consists of series compensator and shunt compensator. The shunt compensator is controlled by a PWM current control algorithm, while the series converter is controlled by a PWM voltage control algorithm. According to the adopted control scheme, these two parts of Nine Switch UPQC have different functions as follows:

4.1 Static Shunt Compensator

In Figure.2 the instantaneous current of the nonlinear load i_L is expanded into 3 terms. The first term i_{Ljp} is the load functions sent from PLL (Phase Locked Loop) in accordance with equation.(3)

$$I_{Ldq0} = T_{abc}^{dq0} i_{Labc} \quad (3)$$

By this transform, the fundamental positive sequence components are transformed into dc Quantities in d and q axes, which can easily be extracted by low-pass, filter (LPF).

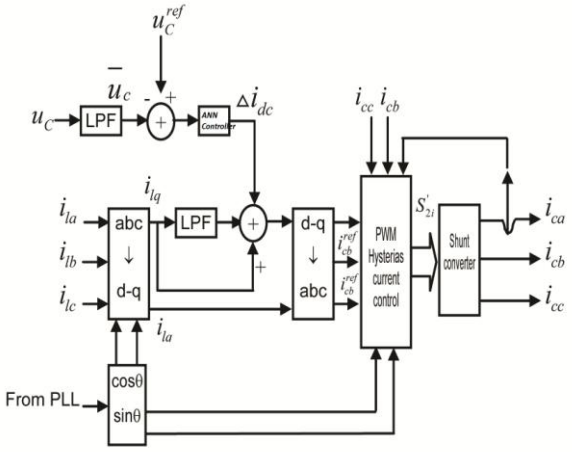

Figure.4 Control of the shunt Converter of the Nine Switch UPQC

All harmonic components are transformed into ac quantities with a fundamental frequency shift.

$$I_{Lq} = \bar{i}_{Lq} + \tilde{\tilde{i}}_{Lq} \quad (4)$$

Since $i_L = i_s + i_c$ (5)

$$U_{sdq0} = T_{abc}^{dqo} U_{sabc} = U_{sLp} + U_{sLn} + U_{sL0} + U_{sh} \quad \ldots(6)$$

This means there is no harmonics and reactive components in the system currents. The switching loss can cause the dc link capacitor voltage to decrease. Other disturbances, such as unbalances and sudden variations of loads can also cause this voltage to fluctuate. In order to avoid this, in Figure 4. a PI controller is used. The input of the PI controller is the error between the actual capacitor voltage and the

desired value, its output then added to the reference current component in the d-axis to form a new U_{sdqo} in control strategy of UPQC

4.2 Static Series Compensator

The system side voltage may contain negative-zero-sequence as well as harmonics components which need to be eliminated by the series compensator [15-16]. The control of the series compensator is shown in Figure.5. The system voltages are detected then transformed into synchronous dq-0 reference frame using equation (6).

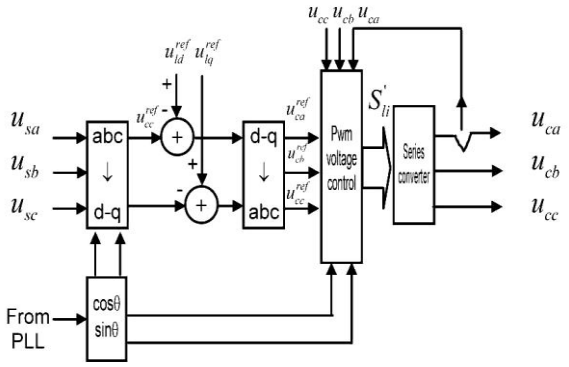

Figure.5 Control block diagram of the series converter of the UPQC.

V. DESIGNING & TRAINING OF ANN

An ANN is essentially a cluster of suitably interconnected non-linear elements of very simple form that possess the ability of learning and adaptation. These networks are characterized by their topology, the way in which they communicate with their environment, the manner in which they are trained and their ability to process information [18]. Their ease of use, inherent reliability and fault tolerance has made ANNs a viable medium for control. An alternative to fuzzy controllers in many cases, neural controllers share the need to replace hard controllers with intelligent controllers in order to increase control quality [19]. A feed forward neural network works as compensation signal generator. This network is designed with three layers. The input layer with seven neurons, the hidden layer with 21 and the output layer with 3 neurons. Activation functions chosen are tan sigmoidal and pure linear in the hidden and output layers respectively.

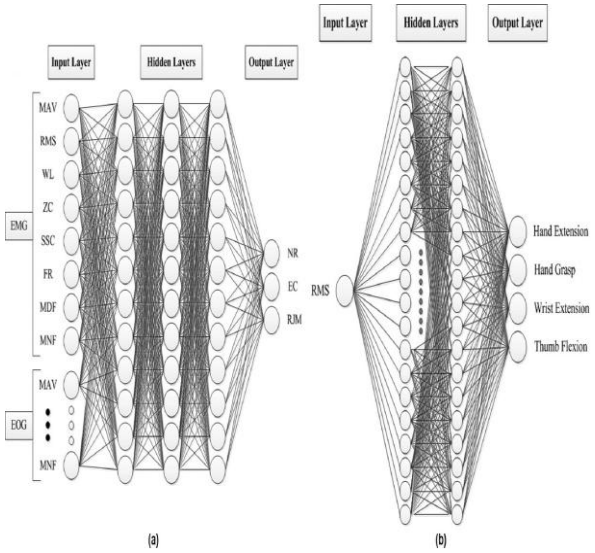

Figure.6.Network Topology of ANN

The training algorithm used is Levenberg Marquardt back propagation (LMBP). The Matlab programming of ANN training is as given below:

```
net=newff(minmax(P),[7,21,3],
{'tansig', 'tansig', 'purelin'}, 'trainlm');
net.trainParam.show = 50;
net.trainParam.lr = .05;
net.trainParam.mc = 0.95;
net.trainParam.lr_inc = 1.9;
net.trainParam.lr_dec = 0.15;
net.trainParam.epochs = 1000;
net.trainParam.goal = 1e-6;
[net,tr]=train(net,P,T);
a=sim(net,P);
gensim(net,-1);
```

The compensator output depends on input and its evolution. The chosen configuration has seven inputs three each for reference load voltage and source current respectively, and one for output of error (PI) controller. The neural network trained for outputting fundamental reference currents [20]. The signals thus obtained are compared in a hysteresis band current controller to give switching signals. The block diagram of ANN compensator is as shown in Figure 7.

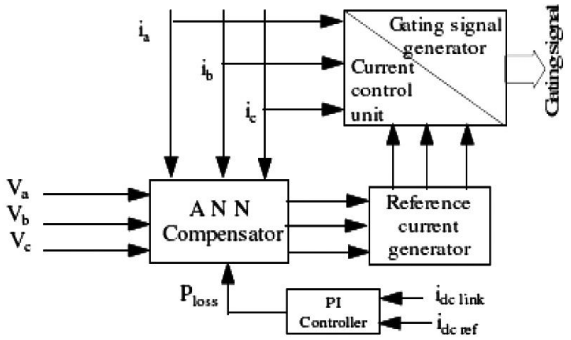

Figure.7 Block diagram of ANN-based compensator

VI. SIMULATION RESULTS

The harmonic content of input and output of the Bridge converter are shown in Figure 8. (three phase voltages) and Figure 9. (three phase currents). due to non-linear loads, such as large thyristor power converters, rectifiers, voltage and current flickering due to arc in arc furnaces, sag and swell due to the switching of the loads etc. One of the many solutions is the use of a combined system of shunt and active series filters like Nine Switch Unified power quality conditioner (UPQC).

This device combines a shunt active filter together with a series active filter in a back-to-back configuration, to simultaneously compensate the supply voltage and the load current or to mitigate any type of voltage and current fluctuations and power factor correction in a power distribution network. The control strategies used here are based on PI & ANN controller of the Nine Switch UPQC in detail. The control strategies are modeled using MATLAB/SIMULINK. The simulation results are listed in comparison of different control strategies are shown in figures.

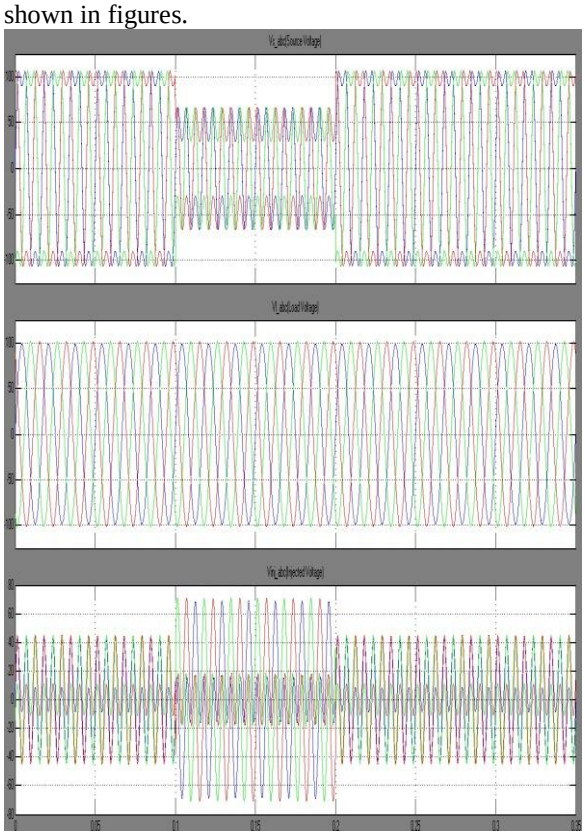

Fig.8.input Voltage, Load Voltage and Injected Voltage with sag condition

Fig.9.input current, Load current and Injected current with sag condition using unbalanced load

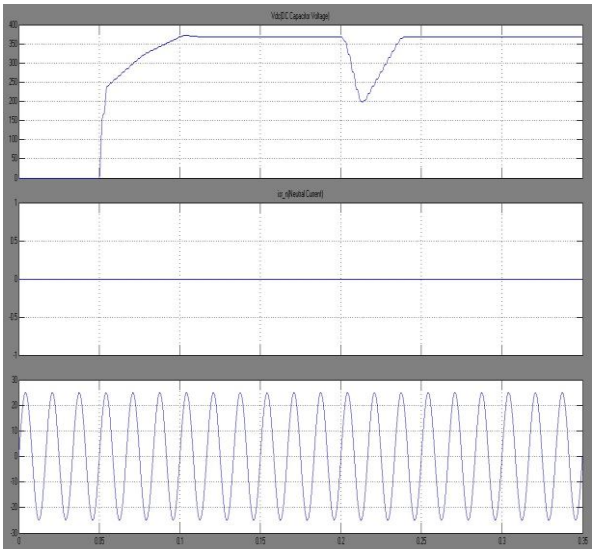

Fig.10.Dc voltage, Neutral compensation current and without compensation

To verify the operating performance of the proposed Nine Switch UPQC, a 3-Φ electrical system, a PLL extraction circuit with hysteresis controlled Nine Switch UPQC is simulated using MATLAB software. Figure 10. Shows the unit vector templates generated by using proposed control technique.

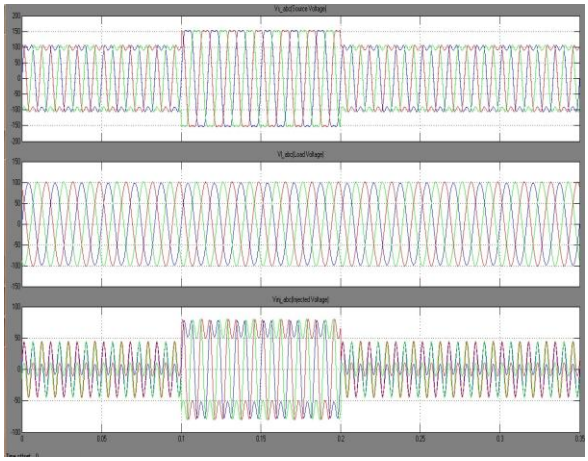

Fig.11.input Voltage, Load Voltage and Injected Voltage with Swell condition

Order of harmonics	WITHOUT UPQC utility side voltage	WITHOUT UPQC utility side current	UPQC with PI controller utility side voltage	UPQC with PI controller utility side current	UPQC with ANN controller utility side voltage	UPQC with ANN controller Utility side current
3rd &5th	4.2	24.2	2.99	2.99	1.2	1.2
5th & 7th	4.2	24.6	3.42	3.42	1.19	1.19
7th &9th	4.2	24.6	2.18	2.18	1.3	1.3

Table.1 Voltage and current harmonics (THD□s) of Nine Switch UPQC

The shunt APF is put into the operation at instant '0.2 sec'. Within the very short time period the shunt APF maintained the dc link voltage at constant level as shown in Figure.13. In addition to this the shunt APF also helps in compensating the current harmonics generated by the nonlinear load. It is evident that before time '0.1 sec', as load voltage is distorted, As soon as the series APF put in to operation at '0.1 sec' the load current profile is also improved. Before time '0.2 sec', the source current is equal to load current. But after time '0.2 sec', when shunt APF starts maintaining dc link voltage it injects the compensating current in such a way that the source current becomes sinusoidal .Current injected by the shunt APF is shown in Figure.12. model of the Nine Switch UPQC has been developed with different shunt controllers (PI and ANN) and simulated results.

VII. CONCLUSIONS

The closed loop control schemes of direct current control, for the proposed Nine Switch UPQC have been described. A suitable mathematical have been described which establishes the fact that in both the cases the compensation is done but the response of ANN controller is faster and the THD is minimum for the both the voltage and current which is evident from the plots and comparison Table.1. Proposed model for the Nine Switch UPQC is to compensate input voltage harmonics and current harmonics caused by non-linear load. The work can be extended to compensate the supply voltage and load current imperfections such as sags, swells, interruptions, voltage imbalance, flicker, and current unbalance. Proposed Nine Switch UPQC can be implemented using simple analog hardware, because it is having PLL and Hysteresis blocks.

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